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(54) Title: MICROCHANNEL COOLING OF HIGH POWER SEMICONDUCTOR DEVICES

(57) Abstract

Cooling of densely packaged semiconductor devices is achieved by microchannels which extract heat by forced convection and the use of fluid coolant located as close as possible to the heat source. The microchannels maximize heat sink surface area and provide improved heat transfer coefficients, thereby allowing a higher power density of semiconductor devices without increasing junction temperature or decreasing reliability. In its preferred embodiment, a plurality of microchannels are formed directly in the substrate portion of a silicon or silicon carbide chip or die mounted on a ground plane element of a circuit board and where a liquid coolant is fed to and from the microchannels through the ground plane. The microchannels comprise a plurality of closed-ended slots or grooves of generally rectangular cross section. Fabrication methods include deposition and etching, lift-off processing, micromachining and laser cutting techniques.

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MICROCHANNEL COOLING OF HIGH POWER SEMICONDUCTOR DEVICES

Background of the Invention

Field of the Invention

This invention relates to convection cooling of high power semiconductor devices and more particularly to microchannel cooling of semiconductor devices formed on a chip of semiconductor material including silicon and silicon carbide.

Description of the Prior Art

As the state of the art of semiconductor technology advances and more particularly to those types of devices which are known as power semiconductor devices, and the circuitry associated therewith, there is a continued demand that such devices operate faster and handle more power, while being ever smaller and lower in cost. The semiconductor industry has responded with the development of integrated circuit chips including thereon a large number of transistor devices such as bipolar transistors including power switching devices such as insulated gate bipolar transistors which are particularly applicable for use in medium to high power (1 to 100kW or more) power converters. Moreover, these devices are currently being incorporated in densely packaged structures that can handle kilowatts of power.

The greatest limitation in the design of such low cost, light weight, high power devices is providing

reliable cooling of the densely packaged components. Current state of the art electronic packaging techniques typically utilize redundant parts and excess substrate boundary regions as well as operating the electronics at less than their rated values. For example, in transmitters, silicon RF transistors are typically operated below their power output capability and spaced apart from one another by relatively large separation distances in order to keep them cooled to standardized operating temperatures. The maximum device junction temperature of a silicon bipolar transistor, as dictated by system reliability studies, is normally between 125 and 135°C. The same techniques apply to power switching devices.

More recently, the use of silicon as substrates is being replaced by the use of silicon carbide which can tolerate increased operating temperatures. These devices, however, are still limited internally by known power density and thermal considerations. In conventionally cooled power semiconductors, moreover, the heat generated in a silicon substrate is conducted through several layers of material to an air or liquid cooled heat sink.

Summary

Accordingly, it is a primary object of the present invention to provide an improvement in the extraction of heat from electronic components.

It is another object of the invention to provide an improvement in the cooling of semiconductor devices.

It is a further object of the invention to provide an improvement in the cooling of power semiconductor devices which are utilized in densely packaged configurations.

It is yet another object of the invention to

provide an improvement in densely packaged semiconductor by convection cooling.

Briefly, the foregoing objects are achieved by microchannel cooling of densely packaged semiconductor devices which extract heat by forced convection and the use of dense fluids in very small channels located as close as possible to the heat source. This maximizes heat sink surface area and provides improved heat transfer coefficients, thereby allowing a higher power density of semiconductor devices without increasing junction temperature or decreasing reliability. In its preferred embodiment, a plurality of microchannels are formed directly in the substrate portion or die of a silicon or silicon carbide chip mounted on a ground plane element of a circuit board and where a liquid coolant is fed to and from the microchannels through the ground plane. The microchannels comprise a plurality of closed-ended passages of generally rectangular cross section. Fabrication methods include deposition and etching, lift-off processing, micromachining and laser cutting techniques.

Further scope of applicability of the present invention will become apparent from the detailed description given hereinafter. However, it should be understood that the detailed description and specific examples, while indicating preferred embodiments of the invention, are given by way of illustration only, since various changes and modifications within the spirit and scope of the invention will become apparent to those skilled in the art from this detailed description.

Brief Description of the Drawings

The present invention will become more fully understood from the detailed description given

hereinbelow and the accompanying drawings which are given by way of illustration only, and thus are not limitative of the present invention, and wherein:

Figure 1 is a perspective view of a silicon bipolar transistor package in accordance with the known prior art;

Figure 2A is a top plan elevational view of the bipolar transistor package shown in Figure 1;

Figure 2B is a front elevational view of the bipolar transistor package shown in Figure 1;

Figure 3 is an exploded front elevational view of the bipolar transistor package shown in Figure 1 and its associated ground plane and heat sink therefor in accordance with the known prior art;

Figure 4A is a top plan or elevational view of a silicon bipolar transistor package in accordance with a first embodiment of the subject invention;

Figure 4B is a front elevational view of the embodiment shown in Figure 4A;

Figure 4C is a bottom elevational view of the embodiment shown in Figure 4A;

Figure 5A is a sectional view of the embodiment shown in Figure 4B taken along the lines 5-5 thereof;

Figure 5B is a front edge elevational view of the member shown in Figure 5A;

Figure 6 is an enlarged top elevational view of the ceramic substrate included in the embodiment of the invention shown in Figures 4A and 4B;

Figure 7 is a partial cut-away perspective view of the semiconductor chip included in the embodiment shown in Figures 4A-4C and being illustrative of a plurality of convection cooling microchannels formed therein;

Figure 8 is an exploded view of a front elevational view of the embodiment of the invention

shown in Figures 4A-4C mounted on a ground plane including coolant ducts formed therein;

Figure 9 is a perspective view illustrative of a second embodiment of the invention;

Figure 10 is a bottom elevational view of a device such as shown in Figure 9 and being further illustrative of microchannel arrangement formed therein;

Figure 11 is a top elevational view of a ceramic frame for the device shown in Figure 9 and being illustrative of input and output microchannel coolant manifolds with a single input port and two output ports;

Figure 12 is a diagram illustrative of the coolant paths for the embodiment shown in Figure 9;

Figure 13A is a top elevational view of a third embodiment of the subject invention;

Figure 13B is a front elevational view of the embodiment shown in Figure 12A and being illustrative of the fluid input and output ports therefor;

Figure 14 is a diagram illustrative of a first method for forming microchannels in a silicon carbide device;

Figures 15A-15C are diagrams illustrative of a second method for forming microchannels on silicon carbide; and

Figures 16A-16C are diagrams illustrative of a third method for forming microchannels on silicon carbide.

Detailed Description of the Preferred Embodiments

This invention is directed to the concept of the inclusion of a plurality of closed-ended convection cooling microchannels formed directly in the semiconductor chip, also referred to herein as a die, comprised of silicon or silicon carbide on which are

formed a plurality of high power semiconductor devices such as bipolar transistors used for RF amplifier and insulated gate bipolar transistors and diodes used in connection with switching applications such as power converters.

Referring now to the drawings and more particularly to Figures 1 through 3, shown therein is a conventional high power transistor package including a plurality of RF transistors distributed across the top of a silicon or silicon carbide die identified by reference numeral 20 and typically having a dimension of 0.35 in. x 0.035 in. x 0.004 in.

The chip/die 20 is located in a package including a nickel plated copper-tungsten flange 22 on which is located a beryllium oxide (BeO) substrate 24 which is nickel (Ni) plated and screen printed with a suitable metal pattern such as molybdenum-manganese (M_O/M_n) alloy. The substrate 24 supports the chip/die 20. On top of the substrate 24 is located an aluminum oxide (Al_2O_3) window frame and through which a pair of beam leads 28 and 30 project and which couple to leads, not shown, connected to the transistor devices, not shown, formed on the die 20. The flange 22 additionally includes outwardly extending end portions 32 and 34 for connection to external circuitry, not shown, via a pair of U-shaped slots 36 and 38. The flange 22, the substrate 24, the window frame 26 and the leads 28 and 30, are brazed together in one operation using a gold/copper (Ag/Cu) alloy braze which is then gold (Ag) plated to provide a finalized packages. After the die 20 is attached, the semiconductor devices are wire bonded using a gold wedge bonder. A covar lid, not shown, is normally attached to the ceramic window frame 26 to form a hermetically sealed package.

With such a structure, solid state transmitter

designers need only to bolt the device to a ground plane element 40 which may comprise part of a circuit board or another substrate. The element 40 is then bolted to a separate air or liquid cooled heat exchanger shown by reference numeral 42.

Where the number of semiconductor devices on the silicon chip/die comprises, for example, 100 or more silicon bipolar transistors operating at RF frequencies, a large amount of concentrated waste heat is generated which must be dissipated by conduction through several lossy layers and interfaces both within the package and through the ground plane 40 and the heat exchanger 42. Although this packaging approach has been utilized in the past due to its simplicity and low cost, advancement in high power device designs has pushed the requirement for efficient thermal designs beyond conventional packing schemes including that shown in Figures 1-3.

Several design features dictate the thermal properties of these devices. These include the coolant properties and flow rate, the heat exchanger efficiency, the device's substrate interface and the internal device temperature rise. However, coolant type, flow rate and inlet temperatures are often dictated by operating platforms or customer specifications. In addition, a dramatic improvement in a finned type heat exchanger without further pushing flow rate and pressure drop, has not been perfected. The thermal interface between the transistor flange and the substrate ground plane may be improved with solder or conductive epoxy. Unfortunately, this adds considerable system cost in rework and retrofitting. However, up to now, great thermal or electrical efficiency improvements in the transistor package have alluded transistor designers.

Turning attention to the subject invention, thermal improvements can be realized by replacing silicon with silicon carbide. Silicon carbide material is more than a 3 to 1 better thermal conductor than silicon. In conjunction with circuit layout refinements, the thermal impedance within an RF transistor package is decreased by approximately 37%. In addition, silicon carbide permits increased power densities over silicon by offering superior voltage and current performance, thereby enabling higher density circuits that can operate over a wider temperature range. Silicon carbide transistors can operate reliably up to 200°C junction temperature. This increases the allowable temperature Δ between the ambient and the transistor junction by 75°C, thus permitting considerably more heat to be dissipated utilizing conventional packaging and heat removal schemes. With silicon carbide, the maximum heat dissipation of an RF transistor can be increased as much as 2.5 times.

This now leads to a consideration of the preferred embodiments of the invention and which include microchannel heat sink geometries which are fabricated directly in the active device portions of the chip or die on which a plurality of identical semiconductor devices are fabricated so that a liquid convection coolant is brought as close as possible to the heat source, thus eliminating the inefficient thermal gradients through the device, circuit board and heat exchanger.

Referring now to Figures 4 through 8, which is directed to a first embodiment of the invention, Figures 4A-4C depict a microchannel cooled silicon bipolar transistor package including a flange 22', the details of which are further shown in Figures 5A-5B,

including a pair of elongated rectangular recesses 44 and 46 which are spaced relatively close together in mutual parallel alignment. The recesses 46 and 48 comprise coolant manifolds for coolant coupled thereto via an inlet port 48 located at one end of manifold 46 and an output port 50 located at an opposite end of the manifold 44. As shown in Figure 8, a liquid coolant 46 is coupled to and from the ports 48 and 50 by means of coolant ducts 52 and 54 formed in a ground plane member 56. A pair of O-rings 58 and 60 act as seals for the ducts 52 and 54 coupled to the input and output ports 48 and 50.

Contiguous with the top of the flange 22' is a substrate member 24' which is shown by the top elevational view at Figure 6. As shown, the substrate 24' includes a pair of relatively narrow coolant manifold slots 62 and 64 which when the substrate 24' is in place, straddle the coolant manifolds 44 and 46 of the flange 22' lengthwise and thus are coupled thereto along their length such that, for example, slot 62 extends over the manifold 44, while the slot 64 extends over the manifold 46. A silicon bipolar transistor chip/die 20', the details of which are shown in Figure 7, is positioned over the two manifold slots 62 and 64 so that the bottom surface 65 of the chip 20' is fluidly coupled to the manifolds 44 and 46.

As to the structure of the chip/die 20' shown in Figure 7, it is depicted as comprising a relatively long, thin body 63 of semiconductor material of silicon or silicon carbide having a plurality of like or identical semiconductor devices 66 fabricated on the top portion 67 thereof and being arranged in a parallel configuration along the length of the semiconductor body as shown. Along the bottom surface

65 is located a plurality of evenly spaced parallel close-ended microchannels 68 which run transverse to the length of the semiconductor body 63 and in mutual parallel alignment with the semiconductor devices 66. Each microchannel 68 typically comprises a groove 0.004 in. deep by 0.001 in. wide. The length of the microchannels 68 are typically 0.032 in. long, with separation spacings 70 of 0.001 in. When desirable, the microchannel 68 can have a width up to 0.004 in., a depth anywhere from 0.006-0.0010 in. and with a spacing up to 0.003 in.

With such a structural arrangement, the heat generated in the bipolar transistors 66 is transferred through solid upper portion of the chip 20' and the fins 70 of the microchannels by conduction and is thereafter transferred to a liquid coolant 45 flowing through the microchannels 68 to and from the manifolds 44 and 46 through the slots 62 and 64. Suitable coolants 45 for the microchannels 68 include water, ethylene glycol water, poly-alpha-olefin, silicate ester, and "Fluorinert" brand liquids, e.g. FC-70, manufactured by the 3M Company.

The use of the very narrow channels or microchannels 68 directly in the chip 20' enhances heat transfer in two ways. First, narrow channels can be closely spaced, providing a large number of fins with a combined surface area much greater than the "foot print" of a conventional heat sink. In addition, the small hydraulic dimensions of the narrow passages provided by the microchannels 68 result in relatively high convection heat transfer coefficients. Since the thermal conductance of a heat sink is proportional to the product of the convective heat transfer coefficient and the surface area, the microchannels 68 permit an increase in the maximum

power density for a given operating temperature. The small size of the microchannel heat sink is thus ideal for direct cooling of hot semiconductor components. The thermal efficiencies in large mass typical with traditional heat transferred from a device, through a heat spreader to a heat exchanger are eliminated. Also, the superior performance realized by microchannel heat sinks enables minimal flow of coolant to effectively remove heat from a hot device. When compared to traditional packaging techniques, as shown in the following Table I, the scheme shown in Figures 4-7 reduces the thermal impedance between the coolant and the transistor junction of the bipolar transistors 66 shown in Figure 7, by over 30%, while reducing the coolant flow required by over 75%. These improvements break the thermal barriers limiting state of the art transistor circuit density designs and power output capability.

Table I

	Silicon Transistor Conventional Liquid Cooling	Silicon Carbide Transistor Conventional Liquid Cooling	Silicon Carbide Transistor Microchannel Cooling
Device heat dissipation	31 Watts	77 Watts	240 Watts
Device junction temp	125°C	200°C	165°C
Thermal Impedance:			
junction-case	1.28°C/W	0.81°C/W	-
case-substrate interface	0.44°C/W	0.44°C/W	-
substrate fluid	0.61°C/W	0.61°C/W	0.21°C/W*
fluid	0.08°C/W	0.08°C/W	0.27°C/W
total:	2.41°C/W	1.94°C/W	0.48°C/W
Coolant type	60/40EGW	60/40EGW	60/40EGW
Inlet fluid temp.	50°C	50°C	50°C
Fluid flow rate	2gpm	2gpm	0.017gpm(63cc/min)

*device junction-fluid

Referring now to a second embodiment of the invention, reference will now be made to Figures 9-11. Shown thereat is an implementation for microchannel cooling of a die of power switching semiconductor devices such as insulated gate bipolar transistors. The semiconductor structure shown in Figure 9 is shown comprising a silicon chip/die 20'' on which is formed a plurality of insulated gate bipolar transistors (IGBT) having a common upper emitter region 72 and underlying common collector region 74 and respective interdigitated gate electrodes 76. Beneath the collector region 74 is a region 78 containing a plurality of microchannels 68', as further shown in

Figure 10, which is intended to depict the fact that the microchannels 68' are close-ended in the same fashion as the microchannels 68 shown in Figure 7 and that they are also aligned in mutually parallel relationship and of substantially the same size. In the IGBT microchannel structure of Figure 9, however, the depth of the channel 68' is 0.008 in., while being 0.002 in. wide, with a 0.001 spacing which define a set of relatively thin fins 70' in comparison to their 0.008 in. depth dimension. The die 20'' (Figure 10) sits on a ceramic frame 24' which now includes three generally rectangular coolant manifolds 80, 82 and 84 which are spaced apart as shown in Figure 11. The middle manifold 82 comprises a coolant input manifold having a coolant inlet port 86 formed at one end, while the two outer manifolds 80 and 84 comprise output manifolds and including a respective coolant outlet ports 88 and 90 at the opposite end from the inlet port 86. The die 20', moreover, is oriented with respect to the ceramic substrate 24' such that the microchannels 68' are orthogonal to the manifolds 80, 82 and 84. The liquid coolant flow direction is further shown in Figure 12, where both the chip 20' and the ceramic substrate 24' are mounted on a ground plane 56' having a single coolant input duct 92 and two output ducts 94 and 96. Such a configuration operate to keep conduction lengths as short as possible.

Referring now to Figures 13A and 13B, shown thereat is a cooling architecture for a third embodiment of the invention which includes the incorporation of fast, soft recovery back diodes connected across a set of IGBT devices in a three phase IGBT power bridge module which can be used, for example, in electric motor control. As shown in

Figure 13A, six IGBT dies $20_1''$ ... $26_6''$ each having single inlet ports 86 and dual outlet ports are positioned next to six back diode dies 21_1 ... 21_6, each including a single inlet port 98 and a single outlet port 100. A single coolant inlet duct 102 is connected at one end to the underside 103 of the ceramic substrate 24''. The substrate is also configured to include a U-shaped inlet coolant manifold 104 having an inlet port 106 formed in the curved end portion thereof. A single coolant outlet duct 108 is connected to the underside 103 at the other end of the ceramic substrate 24'' where it connects to a single elongated coolant manifold 110 which runs down the center of the substrate 24'' between the arms of the inlet manifold 104. An output port 112 connects the coolant outlet manifold 110 to the output duct 108.

The embodiments of the invention thus disclosed having improved heat transfer coefficients permit increased power density with fewer devices, fewer circuits and fewer assemblies when compared to conventionally cooled units delivering the same level of power.

Referring now to Figures 14 through 16, shown thereat are three fabrication techniques for forming microchannels 68 in semiconductor substrates and more particularly silicon carbide. As shown in Figure 14, the simplest way for forming microchannels 68 is simply to use a micromachining process such as saw cutting, into the back of a silicon carbide substrate 20. This technique eliminates any thermal expansion mismatch issues between the silicon carbide and any deposited channel material. The channels can also be formed by using well known laser cutting techniques.

Another approach to the formation of

microchannels 68 on a silicon carbide substrate 20 is to utilize a deposition and etching process shown in Figures 15A-15C. As shown in Figure 15A, a layer of semiconductor or metal alloy material 114, with adequate thermal conductivity and suitable thermal expansion, is built up on one side 21 of a wafer 20 using either deposition or plating. Silicon comprises a suitable semiconductor material. A metal candidate is tungsten. Next as shown in Figure 15B using photolithographic techniques, the material 114 is then etched to form the microchannels 68. Following this and as shown in Figure 15C, a layer of high conductivity material 116 is then deposited on all surfaces of the microchannel 68 as well as the residual material 114 to produce a heat sink with microchannels 68 formed therein. The material outer layer of material 116 serves two purposes. It provides an increased electrical drain contact area for the present silicon carbide transistor design, and it also improves the wetting of the coolant to the channel walls for improved thermal performance.

The third fabrication technique comprises a lift-off process shown in Figures 16A-16C. As depicted in Figure 16A, a selected type of lift-off material 116, which may be, for example, photoresist, glass or silicon dioxide, is deposited on the top surface 21 of the silicon carbide substrate 20. The material is then etched so that the remaining geometry has a retrograde profile as shown in Figure 16A, meaning that the bottom of the etch at the surface 118 is wider than at the top. Microchannel material 114 is then deposited over the resultant mesa configuration 115 as shown in Figure 16B. This causes the deposition of items to fall nearly perpendicular to the surface 118 of the silicon carbide. Microchannels

68 are then formed as shown in Figure 16C by etching away the lift-off material 116 and the microchannel material 114 deposited thereon.

Thus what has been shown and described is an innovative packaging technique and fabrication process for implementing microchannel cooling which will provide thermal efficiency improvements required for compact, high power transistor and/or integrated circuit designs, particularly circuits formed on silicon and silicon carbide.

The invention being thus described, it will be obvious that the same may be varied in many ways. Such variations are not to be regarded as a departure from the spirit and scope of the invention, and all such modifications as would be obvious to one skilled in the art are intended to be included within the scope of the following claims.

CLAIMS

1. A microchannel cooled semiconductor structure, comprising:

a body of semiconductor material;

at least one semiconductor device formed in one region of said body of semiconductor material; and

a plurality of close-ended forced convection cooling microchannel slots formed in another region of said body of semiconductor material.

2. A structure according to claim 1 wherein said body of semiconductor material comprises a die of silicon or silicon carbide.

3. A structure according to claim 2 wherein said at least one semiconductor device comprises a plurality of semiconductor devices.

4. A structure according to claim 3 wherein said plurality of semiconductor devices are formed on an upper region of said die of semiconductor material and said plurality of microchannel slots are formed beneath said semiconductor devices in a lower region of said die of semiconductor material.

5. A structure according to claim 4 wherein said microchannel slots have a width ranging between about

0.001 in. and about 0.004 in., a depth ranging between about 0.004 in. and about 0.01 in., and a spacing therebetween ranging between about 0.001 in. and about 0.005 in.

6. A structure according to claim 4 wherein said microchannel slots have a channel length ranging between about 0.032 in. and 0.5 in.

7. A structure according to claim 4 wherein said microchannel slots are arranged in mutual parallel relationship.

8. A structure according to claim 4 wherein said plurality of semiconductor devices are also arranged in mutually parallel relationship.

9. A structure according to claim 4 wherein said microchannel slots are aligned in parallel with said plurality of semiconductor devices.

10. A structure according to claim 4 wherein said die of semiconductor material is located on support means including means for coupling a fluid coolant to and from said microchannel slots.

11. A structure according to claim 10 wherein said fluid coolant comprises a liquid coolant.

12. A structure according to claim 11 wherein said support means includes a generally flat mounting flange including a plurality of coolant manifolds located adjacent and transverse to said microchannel slots for supplying said coolant to and receiving said coolant from said microchannel slots.

13. A structure according to claim 12 wherein said plurality of coolant manifolds comprises a pair of elongated mutually parallel recesses formed in said mounting flange.

14. A structure according to claim 13 and additionally including a substrate member located between said die and said mounting flange.

15. A structure according to claim 14 wherein said substrate member includes a pair of elongated coolant slots located over and in alignment with said pair of coolant manifolds in said mounting flange.

16. A structure according to claim 15 wherein said die, said substrate member and said mounting flange are included in a sealed package.

17. A structure according to claim 11 wherein said support means includes a frame member located on a ground plane including a plurality of coolants ducts formed therein, said frame member including a plurality of coolant manifolds coupling said coolant ducts to said microchannel slots.

18. A structure according to claim 17 wherein said plurality of coolant manifolds comprise three coolant manifolds oriented transverse to said microchannel slots for supplying said coolant to and receiving said coolant from said microchannel slots.

19. A structure according to claim 11 wherein said support means includes a substrate member having a U-shaped coolant manifold and an elongated straight coolant manifold located within said U-shaped coolant

manifold for supplying coolant to and receiving coolant from said microchannel slots.

20. A structure according to claim 11 wherein said semiconductor devices are comprised of a plurality of transistors.

21. A structure according to claim 20 wherein said plurality of transistors comprise a plurality of RF transistors.

22. A structure according to claim 21 wherein said RF transistors comprise bipolar transistors.

23. A structure according to claim 20 wherein said plurality of transistors comprise a plurality of power switching transistors.

24. A structure according to claim 23 wherein said power switching transistors comprise insulated gate bipolar transistors.

25. A method of extracting heat from a solid-state device comprising the steps of:

forming a plurality of microchannels in one region of a semiconductor body including at least one active semiconductor device formed in another region of the same said semiconductor body;

coupling a source of fluid coolant to and from said microchannels;

effecting a flow of said coolant through said microchannels to extract, by forced convection, heat generated by said active semiconductor device.

26. A method according to claim 25 wherein said

fluid coolant comprises a liquid coolant and said at least one active semiconductor device comprises a plurality of active semiconductor devices.

27. A method according to claim 26 wherein said plurality of active semiconductor devices are formed on an upper region of said semiconductor body and said plurality of microchannels are formed beneath said semiconductor devices in a lower region of said semiconductor body.

28. A method according to claim 27 wherein a semiconductor body is located in a package mounted on a ground plane.

29. A method according to claim 28 wherein said coupling step includes coupling said source of fluid coolant through said ground plane and into said package.

30. A method according to claim 27 wherein said microchannels are mutually aligned with said plurality of active semiconductor devices.

31. A method according to claim 30 wherein said microchannels are aligned parallel with said plurality of active semiconductor devices.

32. A method according to claim 27 wherein said microchannels comprise grooves having a width ranging between about 0.001 in. and about 0.004 in., a depth ranging between about 0.004 in. and about 0.01 in. and having a spacing therebetween ranging between about 0.001 in. and about 0.003 in.

33. A method according to claim 32 wherein said microchannels comprise mutually parallel close-ended grooves having a channel length ranging between about 0.032 in. and 0.5 in.

34. A method according to claim 33 wherein said plurality of active semiconductor devices comprise a plurality of transistors.

35. A method of forming a plurality of forced convection cooling microchannels on a heat generating silicon carbide device, comprising the steps of:

forming a wafer or substrate of silicon carbide having at least one generally flat planar surface; and

micromachining a plurality of elongated close-ended mutually parallel microchannel grooves in said flat planar surface, said grooves having a width ranging between about 0.001 in. and about 0.004 in., a depth ranging between about 0.004 in. and about 0.01 in. and having a spacing therebetween ranging between about 0.001 in. and about 0.003 in.

36. A method of forming a plurality of forced convection cooling microchannels on a heat generating silicon carbide device, comprising the steps of:

forming a wafer or substrate of silicon carbide having at least one generally flat planar surface; and

forming a layer of microchannel material of a predetermined thickness on said flat planar surface,

etching said layer of microchannel material to form a plurality of elongated olose-ended mutually parallel microchannel grooves down to said flat planar surface, said grooves having a width ranging between about 0.001 in. and about 0.004 in., a depth ranging between about 0.004 in. and about 0.01 in. and having

a spacing therebetween ranging between about 0.001 in. and about 0.003 in.

37. A method of claim 36 and additionally including the step of depositing a relatively thin layer of electrically conductive material on all surfaces of said grooves.

38. A method according to claim 36 wherein said step of forming a layer of microchannel material comprises depositing or plating a layer of semiconductor on said flat planar surface.

39. A method according to claim 38 wherein said layer of semiconductor comprises silicon carbide.

40. A method according to claim 36 wherein said step of forming a layer of microchannel material comprises depositing or plating a layer of metal or metal alloy on said flat planar surface.

41. A method according to claim 40 wherein said layer of metal comprises tungsten.

42. A method of forming a plurality of forced convection cooling microchannels on a heat generating silicon carbide device, comprising the steps of:

forming a wafer or substrate of silicon carbide having at least one generally flat planar surface;

depositing a layer of lift-off material on said flat planar surface,

etching the layer of lift-off material so as to generate a plurality of elongated mesas having a retrograde profile where the width of said mesas at a lower portion thereof, adjacent said flat planar

surface is relatively narrow compared to the top portion thereof;

depositing a layer of microchannel material over said elongated mesas and the space therebetween; and

etching away said mesas and the layer of microchannel material deposited thereon, thereby leaving a plurality of elongated close-ended mutually parallel microchannel grooves, said grooves having a width ranging between about 0.001 in. and about 0.004 in., a depth ranging between about 0.004 in. and about 0.01 in. and having a spacing therebetween ranging between about 0.001 in. and about 0.003 in.

43. A method according to claim 42 wherein said layer of lift-off material is selected from a group of materials including photoresist, glass, and silicon dioxide.

44. A method according to claim 42 wherein said layer of microchannel material comprises semiconductor material.

45. A method according to claim 43 wherein said semiconductor material comprises silicon.

46. A method according to claim 42 wherein said microchannel material comprises metal or a metal alloy.

47. A method according to claim 45 wherein said metal comprises tungsten.

FIG.1
PRIOR ART

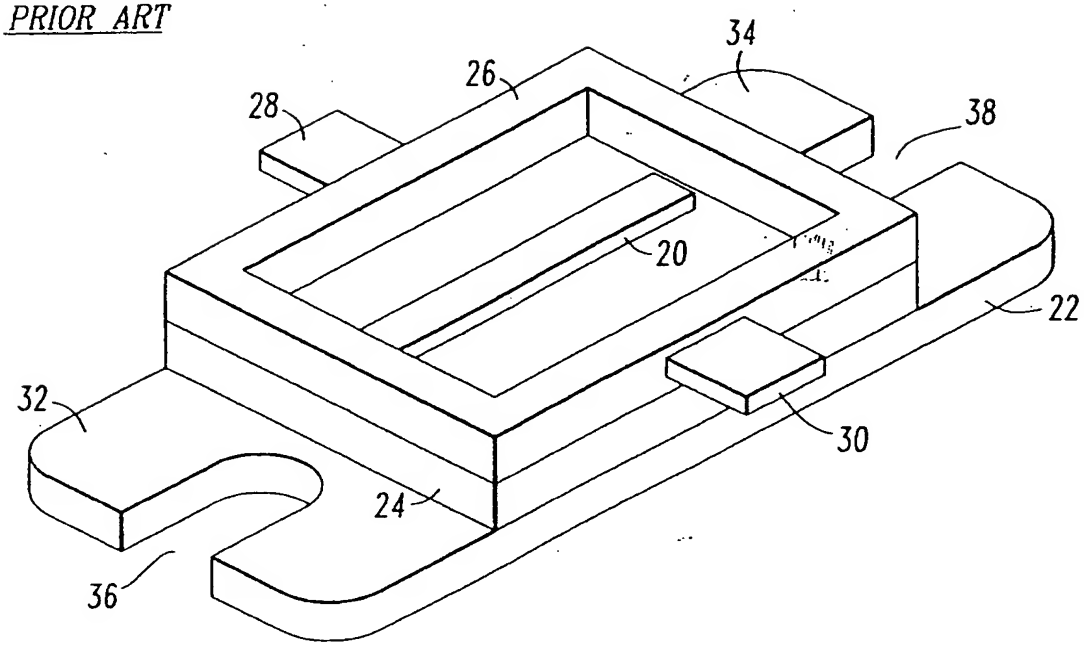


FIG.2A
PRIOR ART

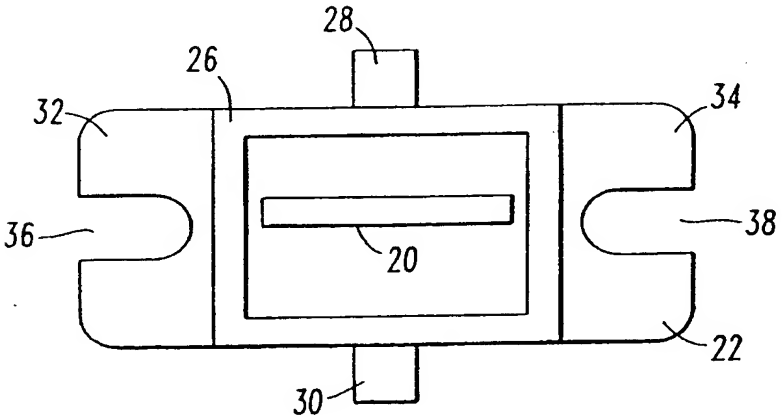
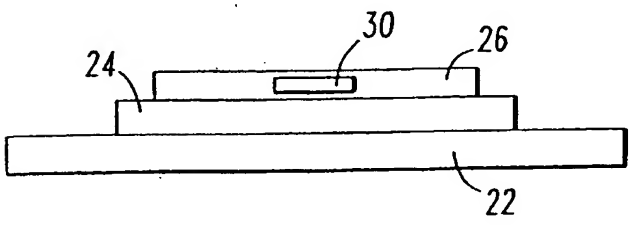


FIG.2B
PRIOR ART



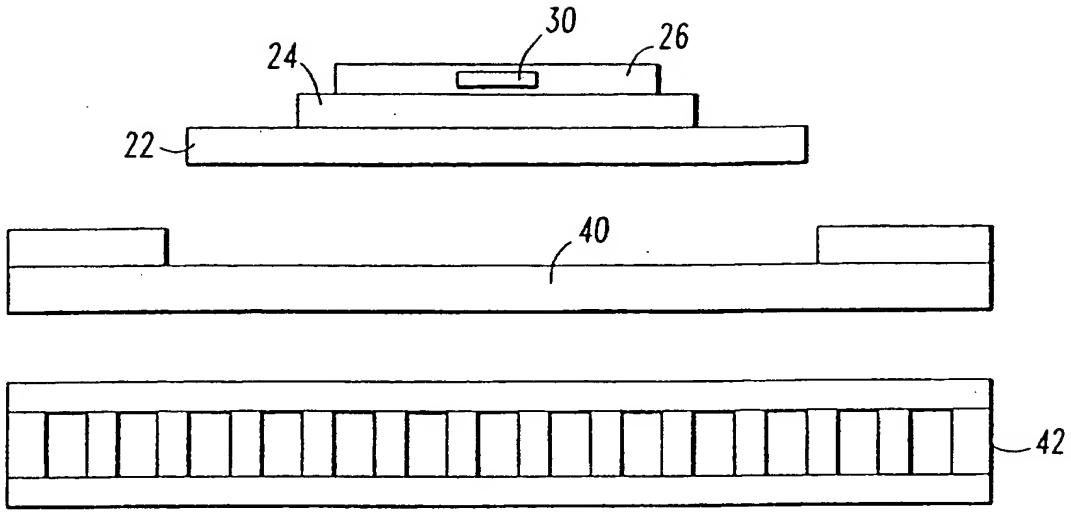


FIG.3
PRIOR ART

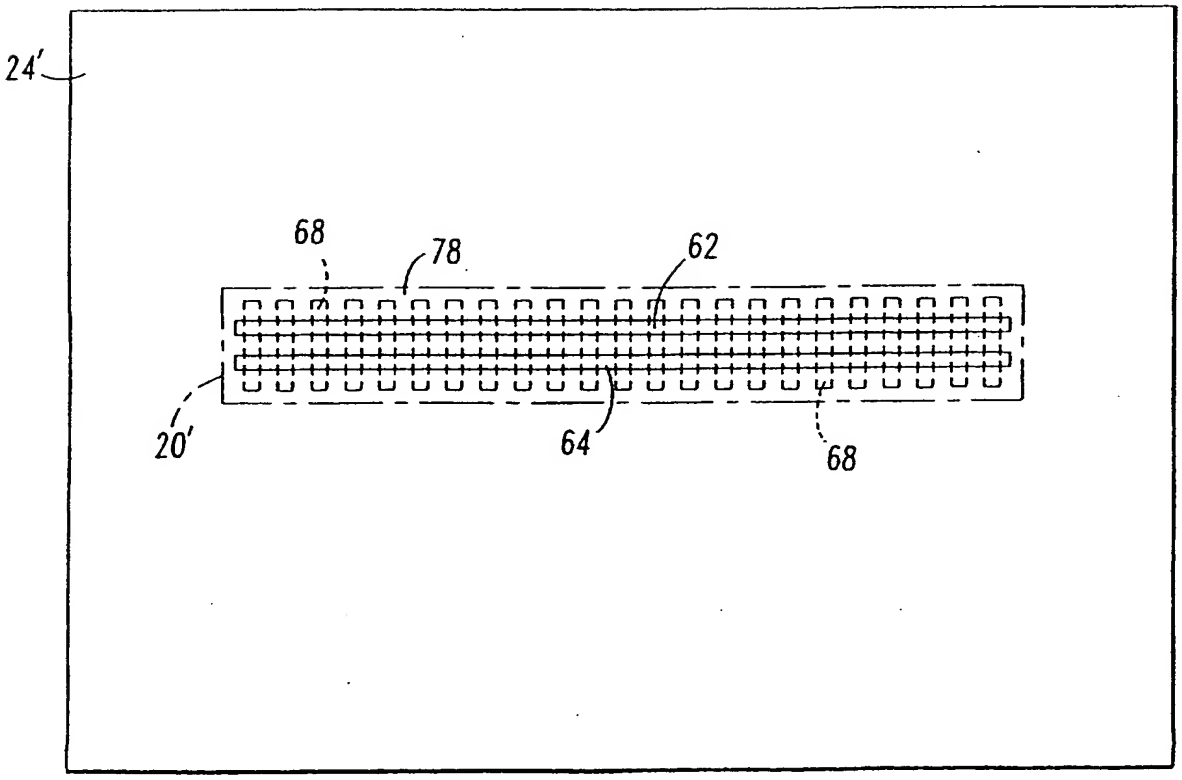


FIG.6

FIG.4A

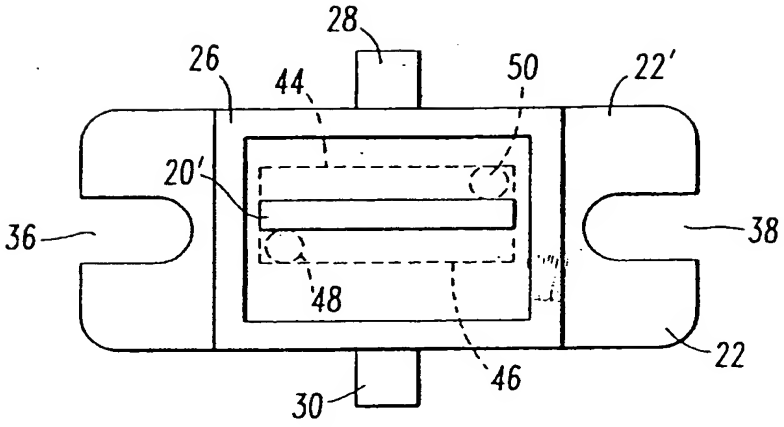


FIG.4B

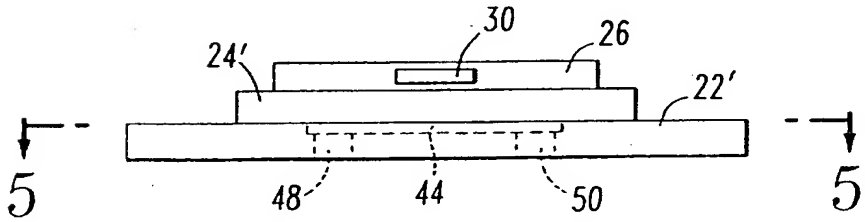


FIG.4C

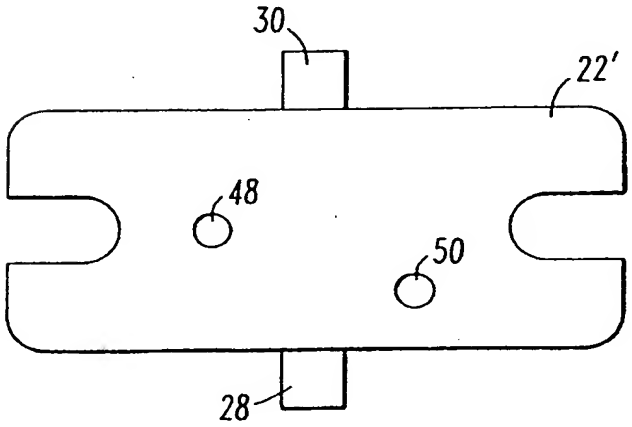


FIG.5A

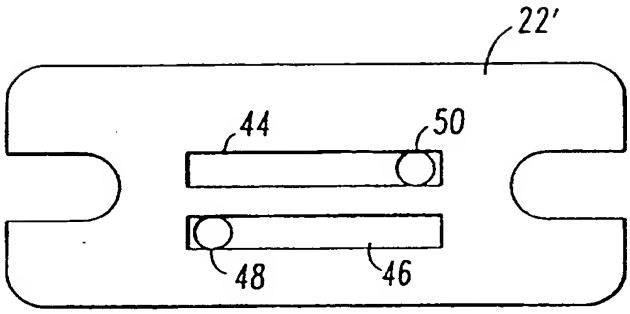
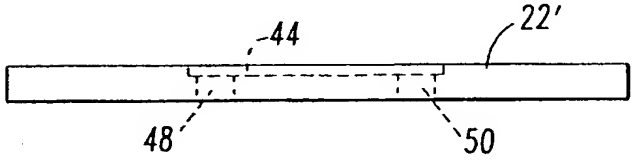


FIG.5B



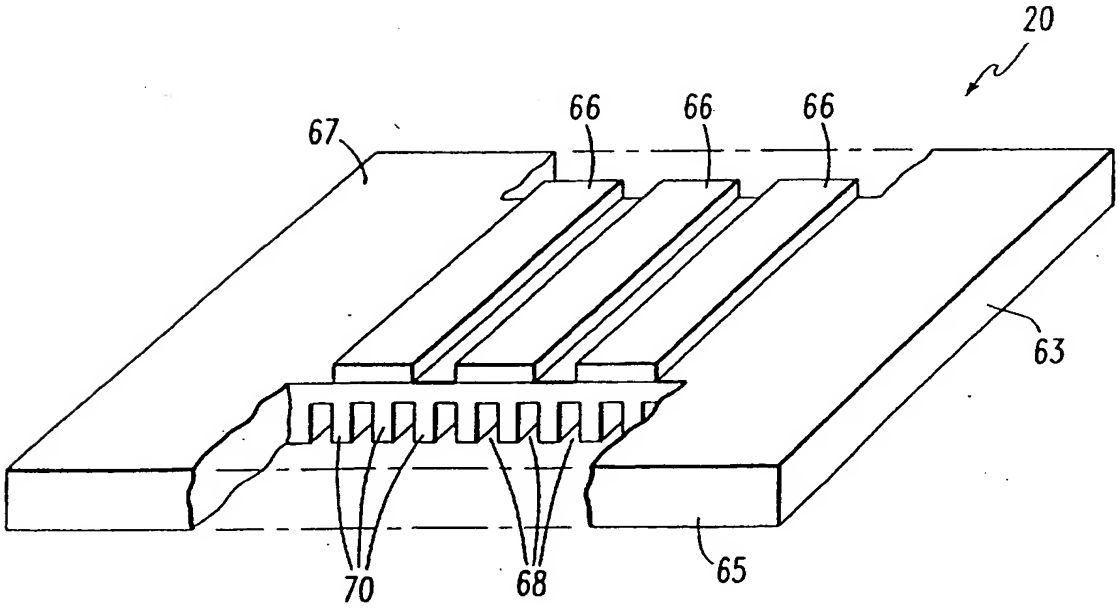
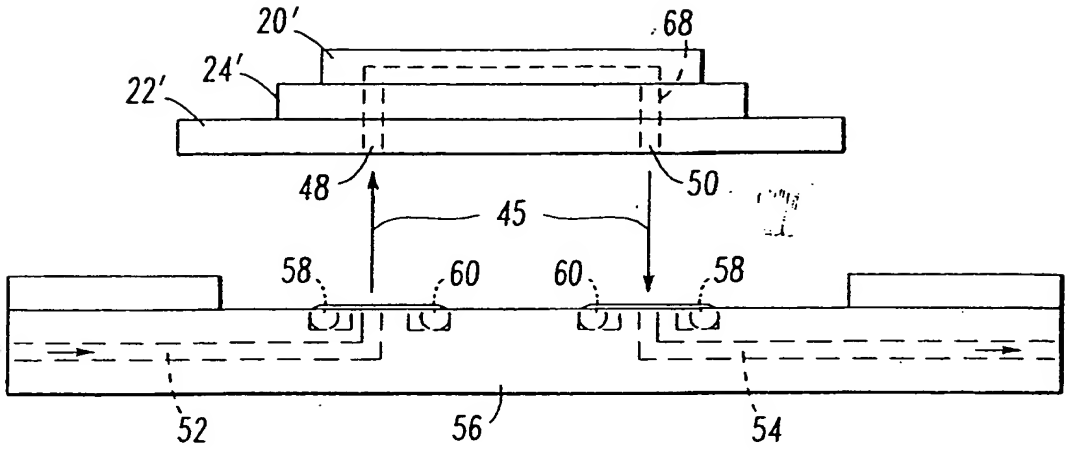


FIG.7

FIG.8



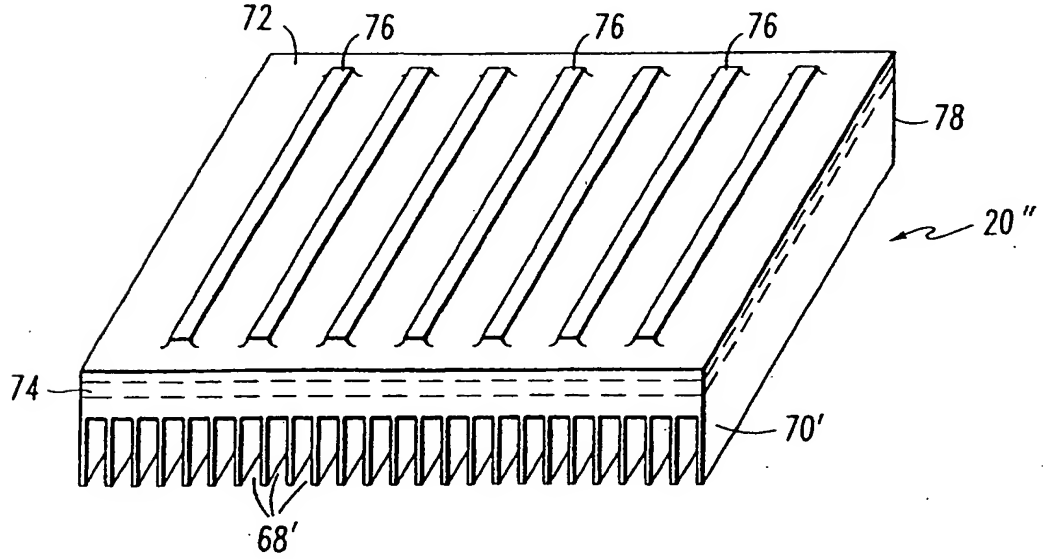


FIG.9

FIG. 10

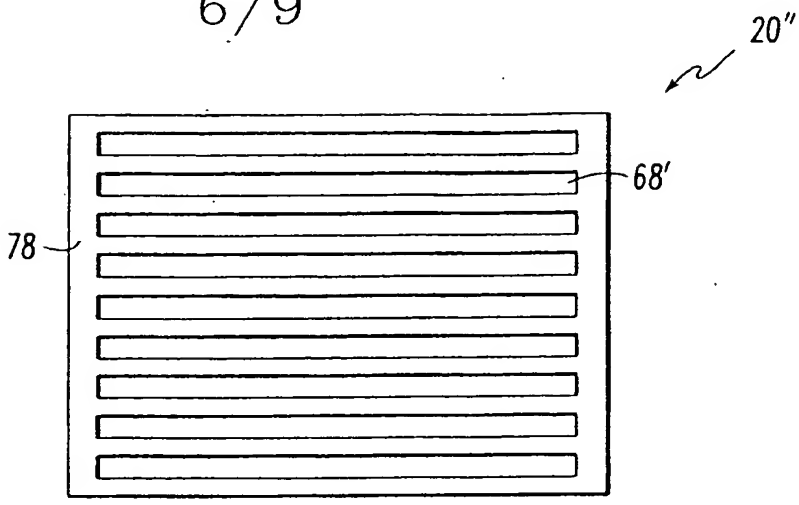
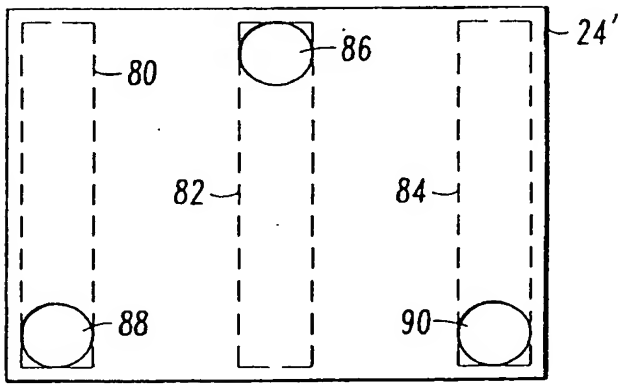


FIG. 11



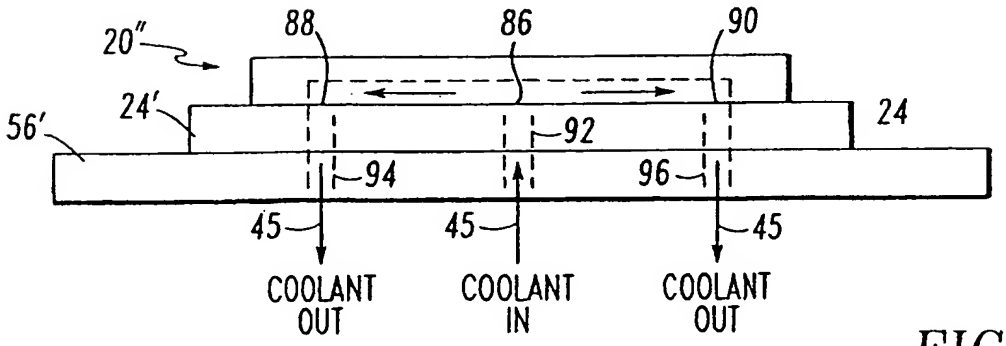
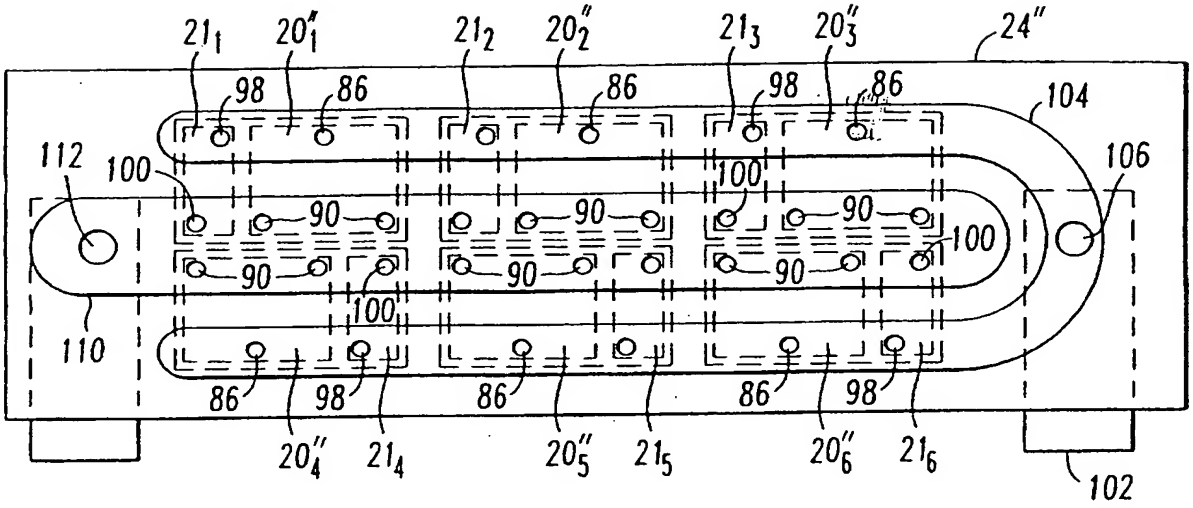


FIG. 12

FIG. 13A



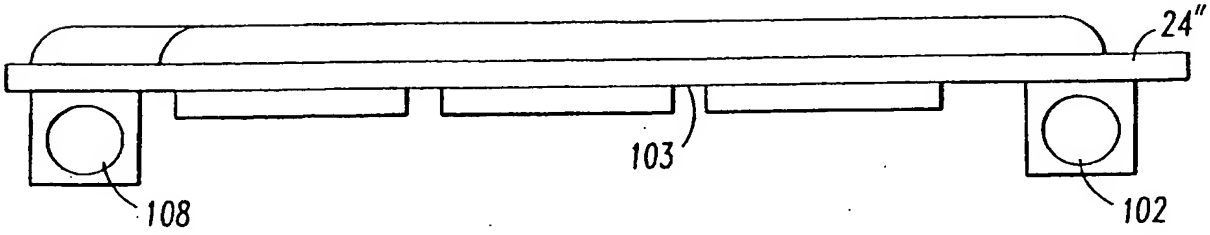


FIG. 13B

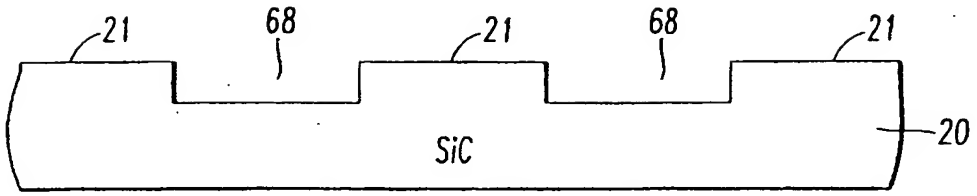


FIG. 14

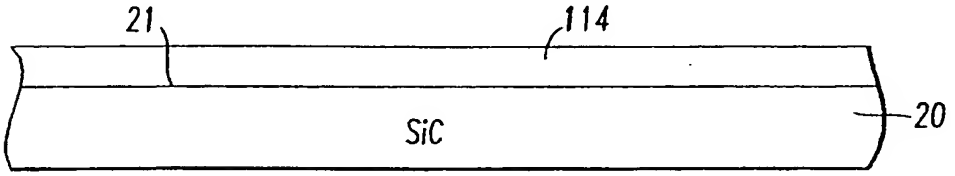


FIG. 15A

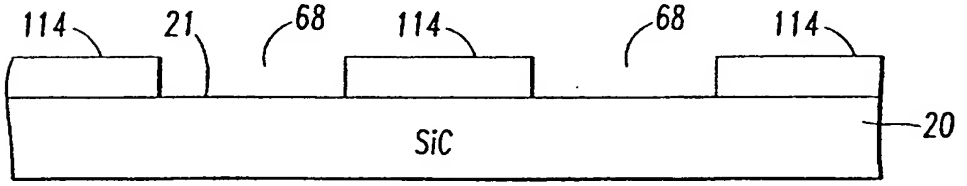


FIG. 15B

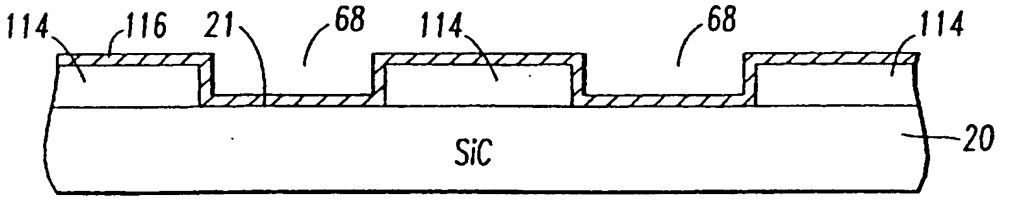


FIG. 15C

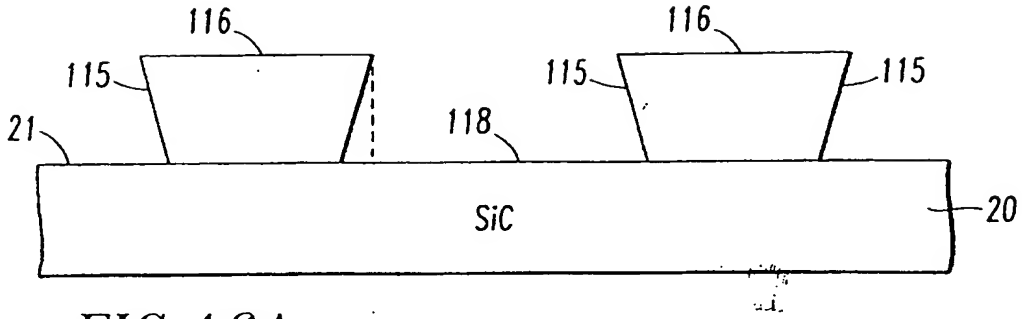


FIG.16A

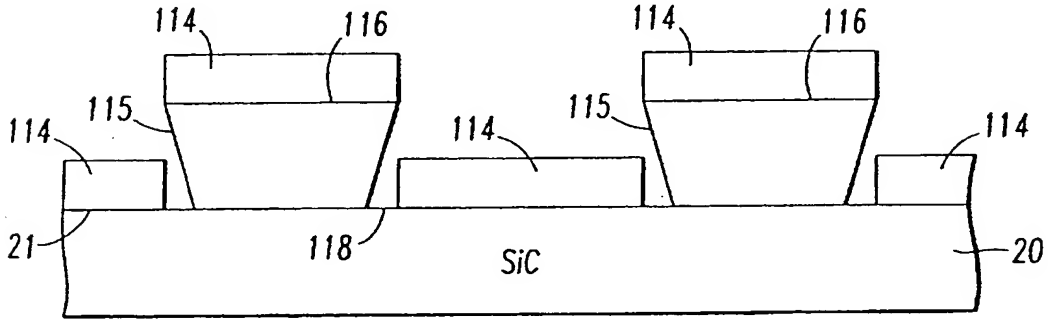


FIG.16B

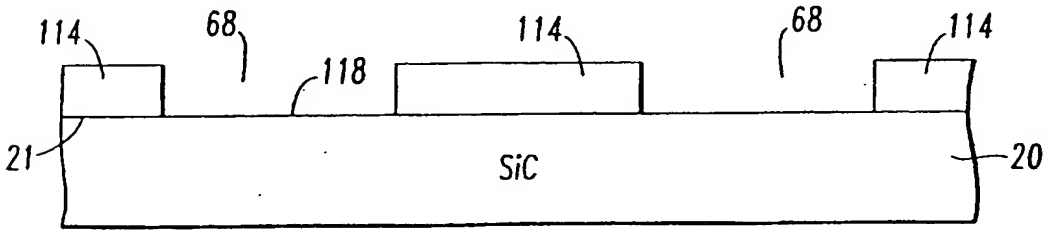


FIG.16C

INTERNATIONAL SEARCH REPORT

Int. onal Application No
PCT/US 97/13316

A. CLASSIFICATION OF SUBJECT MATTER
IPC 6 H01L23/473 H01L23/373

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 6 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 4 450 472 A (TUCKERMAN DAVID B ET AL) 22 May 1984 see column 2, line 32 - column 3, line 46; figures 1-3	1-7,10, 11, 25-27, 32,33
Y	see column 4, line 3 - line 50; figures 5,6	35
A	see column 4, line 59 - line 62	36,42
Y	US 5 251 100 A (FUJITA YUUJI ET AL) 5 October 1993 see column 6, line 9 - line 27; figure 2	35

-/--

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

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"&" document member of the same patent family

1

Date of the actual completion of the international search	Date of mailing of the international search report
9 October 1997	29 -10- 1997

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Le Minh, I

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INTERNATIONAL SEARCH REPORT

Int. ional Application No
PCT/US 97/13316

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 5 241 450 A (BERNHARDT ANTHONY F ET AL) 31 August 1993 see column 7, line 10 - line 46; figure 6	1-4,7, 10,11, 25-27
A	see column 7, line 64 - column 9, line 34; figures 8-12	35,36,42
A	PATENT ABSTRACTS OF JAPAN vol. 011, no. 007 (E-469), 9 January 1987 & JP 61 183949 A (TOSHIBA CORP), 16 August 1986, see abstract	1,25,35, 36,42
A	EP 0 368 743 A (NORTH CAROLINA MICROELECTRON ;IBM (US); NORTHERN TELECOM LTD (CA)) 16 May 1990 see column 9, line 47 - column 10, line 10; figure 1	1,25,35, 36,42
A	LUCHININ V V ET AL: "SILICON CARBIDE MICROTECHNOLOGY" EXTENDED ABSTRACTS, vol. 89 / 2, 1989, PRINCETON, NJ, US, page 706 XP000277116 see the whole document	36,42
A	US 4 771 017 A (TOBIN STEPHEN P ET AL) 13 September 1988 see column 9, line 15 - line 38; claim 8; figures 10-12	42,43, 46,47
A	"METAL LIFT-OFF PROCESS EXTENSION TO SUBMICRON DIMENSIONS" IBM TECHNICAL DISCLOSURE BULLETIN, vol. 30, no. 7, page 203/204 XP000097498 see the whole document	42

1

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INTERNATIONAL SEARCH REPORT

Information on patent family members

Int. Jonal Application No
PCT/US 97/13316

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